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A COUNTERPULSED, SOLID-STATE OPENING SWITCH

by

Michael Graham

June 2005

Thesis Advisor:	William B. Maier II
Co-Adviser:	Richard Harkins

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A COUNTERPULSED, SOLID-STATE OPENING SWITCH

Michael C. Graham
Ensign, United States Naval Reserve
B.S., Physics, United States Naval Academy, 2004

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June 2005

Author: Michael Graham

Approved by: William B. Maier II
Thesis Advisor

Richard Harkins
Co-Advisor

James Luscombe
Chairman, Department of Physics

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ABSTRACT

Railguns have great potential in military roles; however, they currently lack a fieldable power supply. Recent advances in the state of low voltage power storage devices may enable practical Pulse Forming Inductive Network power supplies to be developed if a suitable current interruption device is developed. A solid-state device in a counterpulsed opening switch configuration is a possible solution. A demonstration counterpulsed solid-state opening switch was constructed and successfully tested. This circuit consisted of Silicon Controlled Rectifier components, which can nominally only turn on current. The counterpulsed configuration allowed them to function as opening switches and to do so at much higher current relative to their specifications. We demonstrated current interruption at up to 1 kA of peak current. This demonstration system validates the counterpulsing concept and prepares for the construction of a modular, 250 kJ system.

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I. INTRODUCTION AND BACKGROUND

A. THE RAILGUN POWER PROBLEM

Railguns have real potential to change the nature of fire support on the battlefield. Recently they have begun receiving funding from the Navy; however, they still lack a fieldable power supply. Much work has been done in this area, and several competing technologies have emerged, including high voltage capacitors and rotating machines. Low voltage capacitor and battery technology has historically been of little interest to railgun systems because their energy and power densities were not high, and additional systems are required to boost voltage to railgun operating voltages. Recently, research driven by other industries has advanced the performance of low voltage capacitor by orders of magnitude. Low voltage capacitors are unable directly to drive a railgun, but may be useful in a Pulse Forming Inductive Network (PFIN). While theoretically simple, such a circuit has historically been impractical outside of the lab. Recent advances in low voltage capacitor and battery technology [1] now warrant the reconsideration of PFINs for use in railgun power supplies. Our group aims to show that PFINs can be practically applied in the laboratory and, because of recent advances in capacitor technology, can be developed into a fieldable system. For this thesis, our goal was to demonstrate the concept of counterpulsing on a moderate scale.

B. HISTORICAL USE OF INDUCTIVE SYSTEMS

The use of inductive storage as a component in railgun power supplies is not a novel idea. Some of the first laboratory systems developed in the 1980s used inductors in combination with pulsed alternators to drive some of the first large scale laboratory guns. The 90 mm railgun system at the Center for Electromechanics (CEM) at the University of Texas is a good example of systems from this era [2],[3]. It was constructed with a combination of homopolar generators and inductors. However all these laboratory systems used some sort of single shot switch – usually an explosive switch. Such switching systems are large, inherently dangerous, and thus unsuitable for military applications. The system we propose uses much the same concepts of inductive voltage boosting and pulse shortening, but on a smaller, modular scale. Most importantly, it does not require explosively broken circuits.

C. PFIN SEQUENCE OF OPERATION

A PFIN operates on the basic idea that inductors oppose changes in current. The voltage across an inductor is given by the equation:

$$V = L\frac{\partial I}{\partial t}$$

where t is time, V is the voltage across the inductor, L is the inductance, and I the current through the inductor. Figure 1 shows a simplified schematic of a PFIN.

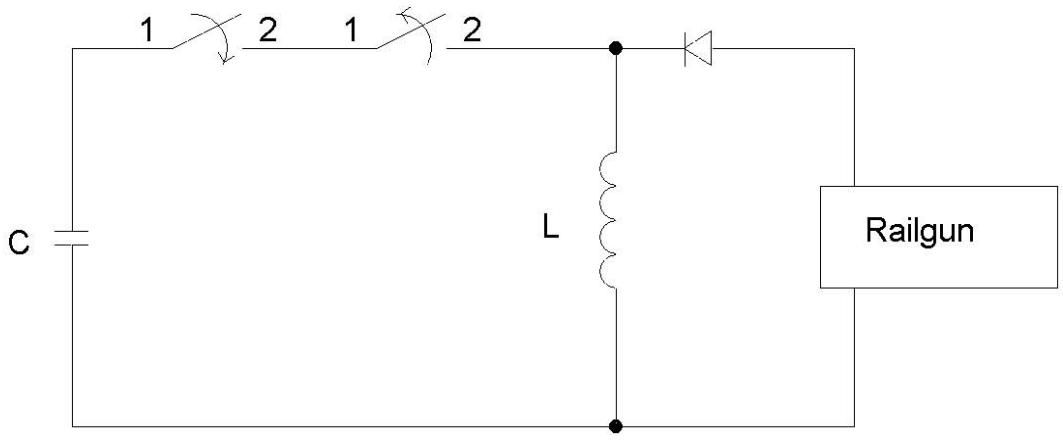

Figure 1. Simplified PFIN Schematic (After: [4])

1. Charging the Inductor[1]

A PFIN's charging phase begins with the closing of the switch, which allows current to flow from the capacitor bank through the storage inductor. Electrostatic potential energy in the capacitor is converted into current and is in turn stored in the inductor as a magnetic field. In the charging phase, the circuit behaves just like an LRC tank circuit since the blocking diode prevents current flow into the railgun load. In a PFIN with sufficiently low resistance, the maximum current occurs at time given by:

$$t_{I_{\max}} \approx \frac{\pi}{2}\sqrt{LC}$$

where L is the inductance of the current loop and C is the capacitance. Figure 2 shows the effective schematic of the PFIN during the charging phase.

[1] Charging is usually associated with batteries or capacitors. For lack of a better term, I call transferring energy into the inductor "charging the inductor" and the process of transferring energy out of the magnetic field of the inductor and into the railgun "discharging the inductor".

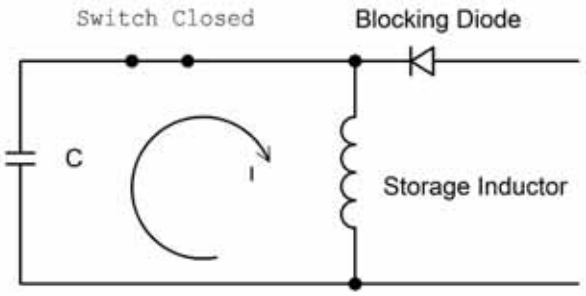

Figure 2. Effective Schematic of Inductor Charging

2. Discharging the Inductor

The discharge phase of PFIN operation begins when the switch opens and halts current flow from the capacitor bank. The inductor responds to this change in current by generating a voltage in the reverse direction from the capacitor bank. Since the voltage is in the reverse direction, current flows through the railgun and the blocking diode. Current continues to flow until the magnetic field in the inductor has collapsed. Figure 3 depicts this phase of PFIN operation.

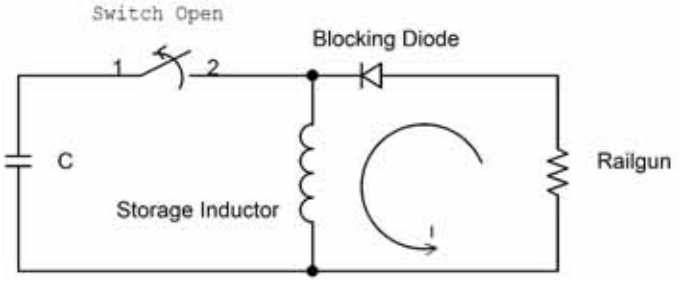

Figure 3. Effective Schematic of Inductor Discharging

D. ADVANTAGES OF PFIN USE

A practical PFIN would have a number of fundamental advantages over competing technologies. Capacitors and inductors require little to no maintenance, and solid-state switching systems are also essentially maintenance free. Low voltage capacitors hold energy for long periods of time with low loss. Failure modes of low voltage capacitors are relatively benign, particularly compared with rotating systems. In a modular system, the stored energy of each module is easily tailored by the charging voltage – an important and flexible consideration in large power supplies where interchangeability is an important factor in system reliability. Multiple designs are not needed for different modules; the pulse characteristics of the system can be changed very

quickly simply through initial voltage and discharge triggering. Different models of capacitor with different working voltages need not be specified in inductive systems.

E. TECHNICAL CHALLENGES

The concept of a PFIN is easy to describe, but the design of a practical one has two stumbling blocks: achieving low resistance and current interruption. Any railgun power supply must achieve low resistance to be practical from a waste heat generation standpoint. But a PFIN also has the requirement that the charging circuit must "resonate" to transfer energy into the storage inductor efficiently, and resistance must be low for resonance to occur. Fortunately, resistance is a straightforward problem to mitigate so long as the resistance of the capacitors or batteries themselves is reasonable. The resistance of the systems 'plumbing' – bus bars, cables, and so forth – can always be lowered by increasing size or using stranded geometries to increase surface area if skin depth is an issue. "Reasonable" is a not a particularly clear quantity; the series resistance of any bank of capacitors can be reduced by placing many in parallel. So a reasonable series resistance value is primarily a function of the overall system size and weight; there is no hard or fast upper bound.

Secondly, a PFIN must by design interrupt or divert very large currents, which is in general a tricky thing, and as such is a primary challenge of any PFIN. Alternating Current (AC) power systems often interrupt large currents (e.g., circuit breakers); however, their situation is different than ours and much easier: AC power systems have zero-current states every 8.3 ms. Arc suppression within the switch is enhanced by the periodic current zeros. In our case, an inductive voltage booster aims to interrupt the current not at a zero crossing, but at the time of maximum current – the very worst time from the switching system's perspective. Consequently, many technologies used in circuit breakers like vacuum and gas filled switches are not necessarily suitable for PFIN use.

F. SOLID-STATE SWITCHES

Explosive switches solved the current diversion problem in laboratory systems but since they are impractical for real world use, we set out to find a better way. We assumed that any inductive system would not be monolithic – a single inductor driving a 200 MJ gun would be untenably sized, and produce the wrong current pulse shape anyway. Any

multiple module system must be well timed with the minimum of jitter to drive a railgun whose total shot time is on the order of 8 ms long. Solid-state switching systems are inherently easier to synchronize than mechanical systems, and they avoid the entire arc-extinguishing problem. As an added benefit, they are maintenance free over a very long lifetime (decades). Because of timing and arc considerations, we decided to use a solid state switching system in our demonstration PFIN.

The problem with using solid-state switches is that they generally can't be used for current interruption at this magnitude. Commercial solid-state opening switches are generally limited to around 4 kA of interrupting current [5], although for quasi-non-repetitive operation, this limit might be stretched. Such devices, used off the shelf, are not attractive for our purposes; the maximum interruption current is an order of magnitude too low to produce a space and weight efficient switching system. Pokryvailo encountered the same problem as part of an inductive system for an ETC gun [6], [7], [8], and devised a novel solution using a combination of vacuum switches and thyristors in an arrangement he called counterpulsing.

G. COUNTERPULSING

A counterpulsing (CP) switch operates by lowering the current through the primary switch for just enough time to shut off the main switch. The primary switch carries current for the entire time before counterpulsing begins (Figure 4). A second, or counterpulsing, switch discharges a counterpulsing capacitor across the primary switch to produce this transient current reduction (Figure 5). The counterpulsing capacitor 'steals' current from the primary switch into the counterpulsing branch. By pulling all the current flow out of the primary switch, the primary switch has enough time for its charge carriers to decay[2] and open (Figure 6). The counterpulsing capacitor is of relatively low capacitance, and since it carries the full load of the main switch, it quickly reverses voltage. This charge stored on the counterpulsing capacitor provides the stopping potential to halt the flow of current out of the capacitor bank (Figure 7). Even if the charge on the main capacitor bank is zero at current shut-off, some inductance is associated with the capacitors themselves and the wiring between the capacitors and the

[2] This sequence describes how our SCR based switch operates. In a system where the primary switch is a turn-off device (e.g. an IGCT or GTO) rather than a circuit-commutated device, the primary switch will close based on the voltage applied to its gate.

switch. So even in a perfectly timed counterpulse operation, residual charge (of opposite polarity to the initial charge of the counterpulsing capacitor and opposing the residual charge on the main capacitor bank) will remain on the counterpulsing capacitor.

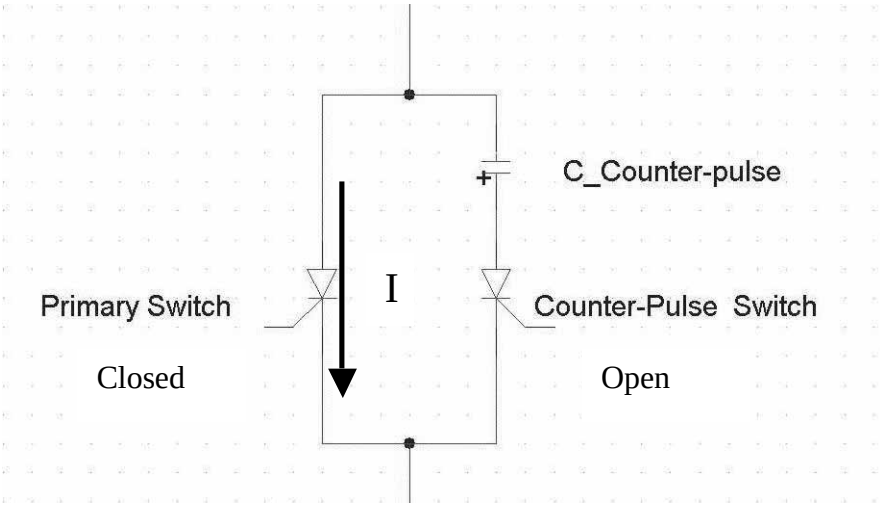

Figure 4. CP Switch Operation – Primary Switch Closed

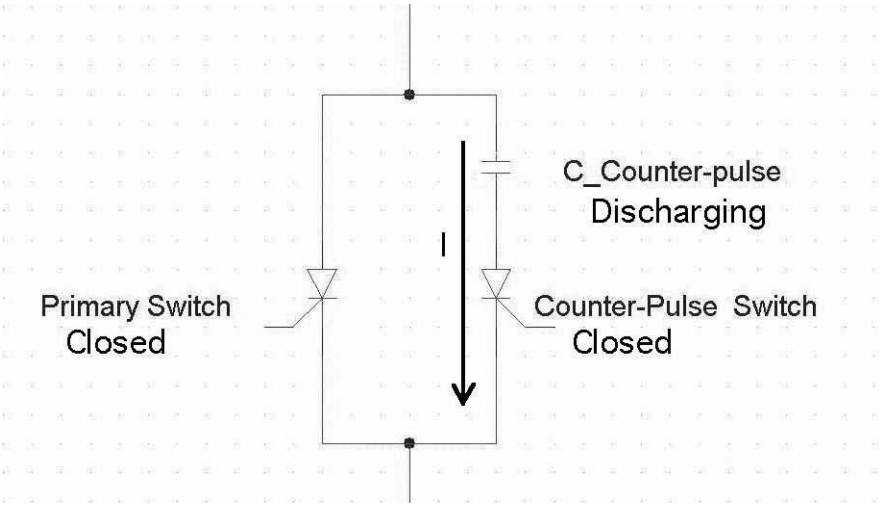

Figure 5. CP Switch Operation – Counterpulsing

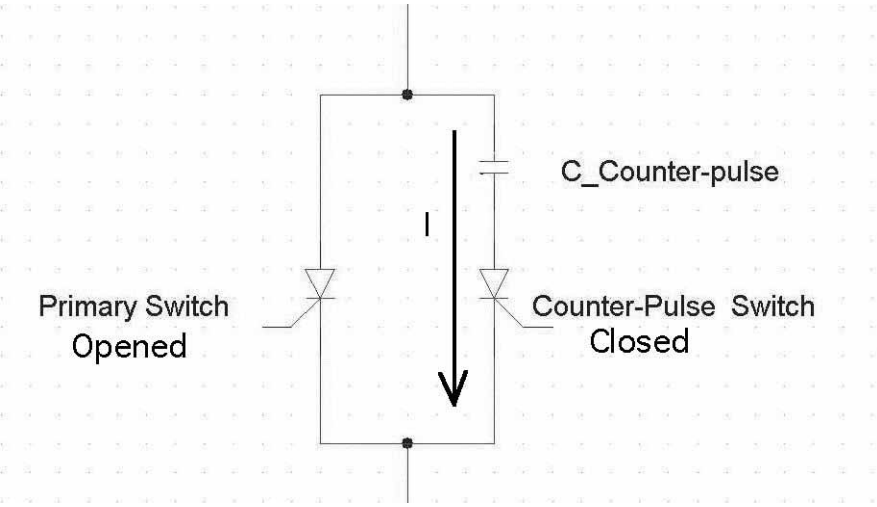

Figure 6. CP Switch Operation – Primary Switch Opens because of no-current state across the Primary Switch.

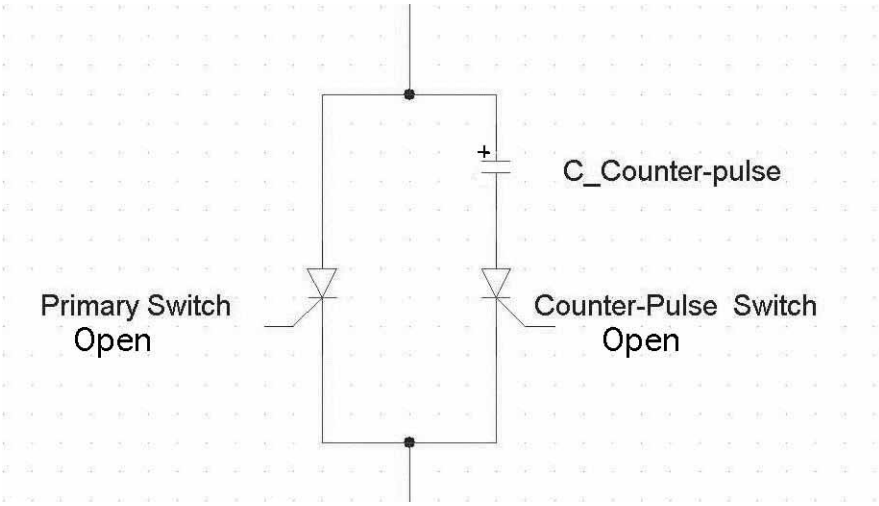

Figure 7. CP Switch Operation – Reverse Charge on CP Capacitor causes current to stop. The no-current state causes the CP Switch to open.

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II. SYSTEM DESIGN

A. GOAL OF SYSTEM

The short term goal of the railgun research group is a PFIN system suitable for a laboratory railgun with an initial electrical storage capacity of 250 kJ. The purpose of this thesis was to demonstrate a counterpulsed, solid-state opening switch. Therefore, the goal of this experiment was the successful operation of a counterpulsed opening switch. Some components of the planned system were used, primarily because they had already been purchased. However, in general the experiment was not a scaled-down model of any future system. The only constraint going into the design process was using 1600 μF capacitors, and a peak current on the order of 1 kA.

B. BASIC SYSTEM DESIGN PARAMETERS

1. Peak Current

The ultimate goal of the 250 kJ system is a peak current per module of approximately 50 kA, since this has been demonstrated for counterpulsed solid-state switches in [6],[7],[8]. For this demonstration, we decided upon a designed peak current of 1 kA. Devices capable of carrying surge currents on the order of kiloamps are easy to obtain and fairly cheap, and 1 kA is within an order and a half of magnitude from our ultimate goal. Additionally, one of the anticipated problems with the counterpulsed switch had to do with stray inductance not within the storage inductor. Such inductance would make opening the switch more difficult. A 1 kA peak current should generate high enough current derivatives to make any such problems apparent.

2. Counterpulsing Considerations

Our demonstrator design departs from our ultimate goal system on a functional level by using a different type of silicon switch. Using SCRs, which are circuit-commutated turn off devices[3], rather than GTOs, which are gate commutated turn off devices, resulted in a fundamentally different turn off mechanism for the main switch. We feel this makes the demonstration problem harder, and thus a more useful demonstration of counterpulsing, since we cannot rely on the main switch to interrupt any

[3] Meaning that they turn-off when the current through them is zero for a length of time (the circuit-commutated turn off time).

current, and must force a zero current or negative current state on the main switch for several tens of microseconds. Nonetheless, it results in our counterpulsing capacitance being larger than it would be in a system in which switches capable of opening are used.

3. Choice of Inductance

Since we were designing a demonstration system and thus more concerned with proper operation instead of transfer efficiency, we chose to use a rather large inductance to stretch out the resonance period of the LRC charging circuit. As a rough entering argument, we desired an inductor charging time of around 1 ms and a peak current of 1 kA. Other constraints were: maximum voltage of main bank limited to 360V. Given these parameters, we chose a main bank capacitance of 7500 μF and an inductance of 44 μH. When charged to 115 volts, an idealized design using these values yields a peak current of 1.5 kA, which is the surge current limit of the SCR components.

C. CHARACTERIZATION OF COMPONENTS

1. Capacitors

When we began the design process, 1600 Cornell-Dubilier model 7P252V360N082 photoflash type electrolytic capacitors had already been purchased for used in the 250 kJ system. They are cylindrical, approximately 40 mm in diameter and approximately 80mm in height. These capacitors have a working voltage of 360V and a nominal capacitance of 2500 μF. The inductance of a single capacitor was low enough to be out of range of an HP 4192A LF Impedance Analyzer. We characterized the inductance to be approximately 23 nH by observing the voltage across the 2500 μF capacitor with respect to frequency in series with a smaller 0.045 μF capacitor driven by a 10 V_{pp} sine function generator. The greatest response was observed at 4.7 MHz, which corresponds to a circuit inductance of 23 nH. Since the physical size of the circuit was small, and the 0.045 μF capacitor was also small, we conclude that the inductance of the 2500 μF capacitor was less than, but very close to, 23 nH. A PSpice simulation of the same circuit also yields a resonant frequency of 4.7 MHz. Figure 8 shows a schematic of the setup, some internal resistances are omitted for clarity, although we considered them in our analysis.

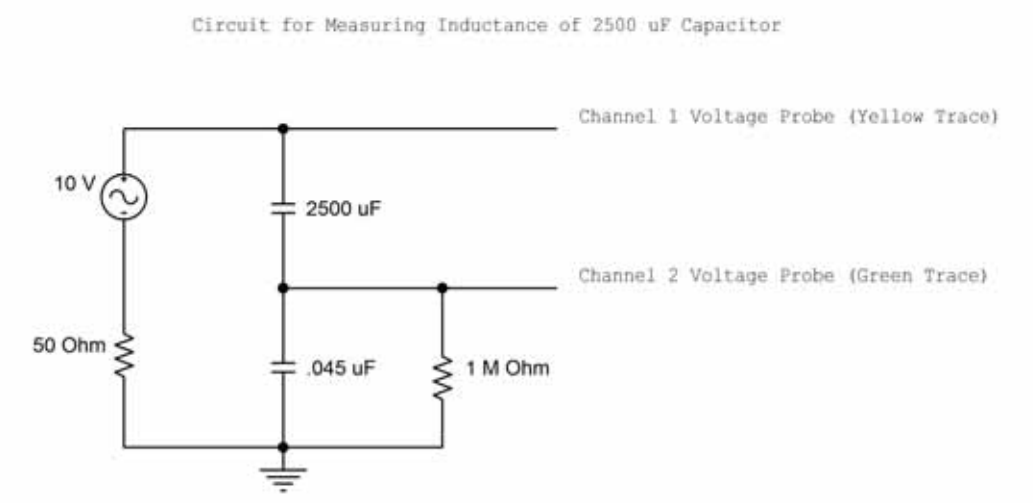

Figure 8. Schematic of circuit used to measure inductance of one 2500 mF capacitor.

2. Sixty Module Capacitor Bank

To assist in designing the first module in our demonstration system, we constructed a notional capacitor module consisting of sixty 2500 μF capacitors in parallel (Figure 9). We used this module to get a general feel for the packing densities, bus work design, and assembly issues of a large parallel bank, as well as electrical performance of a group of our capacitors. We measured the impedance of this 60 capacitor bank in a similar manner to a single capacitor. The schematic for this setup is shown in Figure 10. We drove the bank with a 5 V_{pp} function generator. We placed a 1 μF capacitor in parallel with the 60 capacitor bank and measured the voltage across the capacitor as we swept the drive frequency. Since 150 mF is so much larger than 1 mF, we can idealize the circuit to a simple LC circuit by assuming that all the inductance in the circuit is from the bank. We then observed the resonant frequency of the system and used the ideal LC circuit condition that:

$$\omega = 2\pi f = \frac{1}{\sqrt{LC}}$$

or

$$L = \frac{1}{C(2\pi f)^2}$$

Using this method, we measured the inductance of the 60 capacitor bank to be 40 nH, which is much more than the inductance of sixty 23 nH capacitors in parallel. Therefore, we concluded that the majority of inductance in the bank is due to the inductance of the bus work.

Figure 9. 60 Capacitor Bank

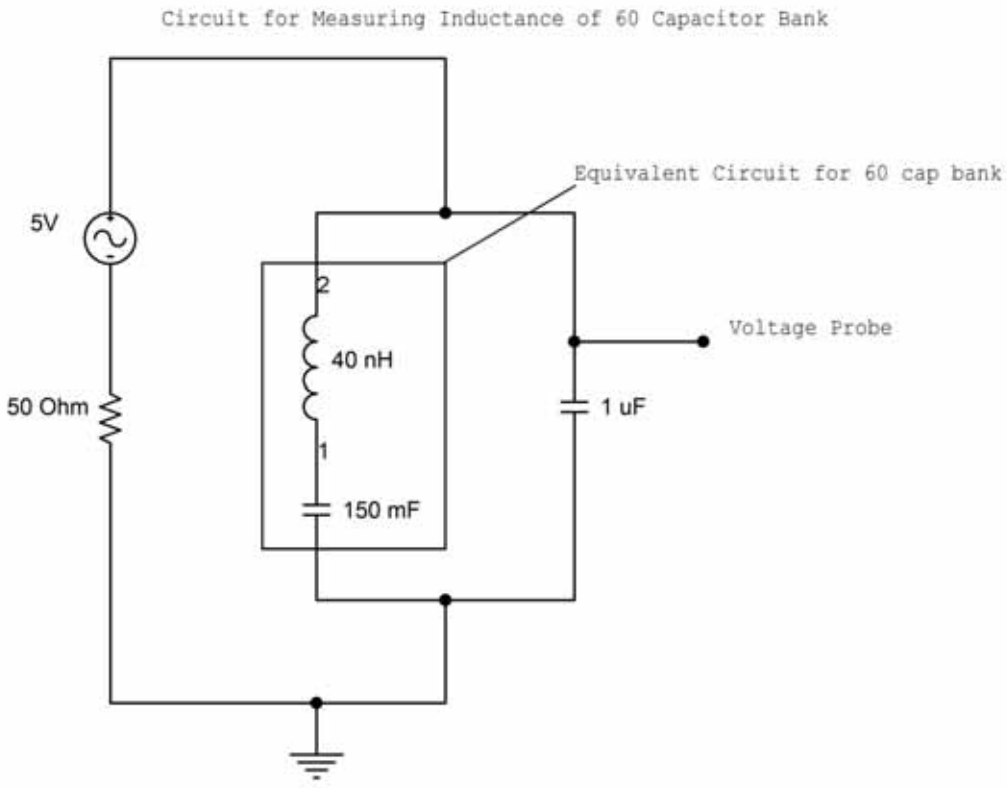

Figure 10. Schematic for Measuring Inductance of 60 Capacitor Bank

3. Silicon Controlled Rectifier

We used NTE 5368 Silicon Controlled Rectifiers (SCR) in our CP demonstration circuit. Table 1 lists some of the more relevant characteristics of the device. As an off the shelf SCR, they are designed to be used primarily in power electronics, but they had a surge current limit high enough meet our design criteria (1.5 kA). As part of our building process, I tested them in a LRC discharge circuit where I observed forward voltages to be on the order of 2 V at currents of 1 kA.

Repetitive Peak Hold-off Voltage	600 V
Average On-State Current	75 A
Peak One-cycle Surge Current	1500 A
Max Surge Energy (3 ms)	10,000 A^2s
Circuit Commutated Turn Off Time	20-40 μs

Table 1. Summary of NTE5368 SCR Characteristics (From: [9])

4. Inductor Design

We used inductor charging time as the primary parameter in inductor design rather than transfer efficiency. As a rule of thumb, we wanted to keep the charging time around 1 ms to assist with counterpulsing. We estimated the required inductance to achieve this charging time using a simple LC circuit. Given a capacitance of 7500 μF, an inductance of 50 μH gives an inductor charging time of 0.9 ms. We elected to use an existing 44 μH inductor simply because it was available. It was oversized – 4/0 gauge wire is much larger than we required – but it was available and sufficient.

5. SCR Triggering

Both SCRs in our demonstration circuit were triggered by 1 ms long square pulses from a Stanford Research delay generator (Model DG-535) after amplification in an in-house designed pulse amplifier. The pulse amplifier converted a 5 V_{pp} square pulse into a 30 V_{pp} pulse and provided much more current than the delay generator, which is designed

to drive a high impedance output at low power. A 1:1 transformer was used to isolate the pulse amplifier from the anode and cathode of the SCRs since both these nodes float to high voltages during operation of the circuit.

D. CIRCUIT MODELING

Besides using basic circuit analysis in the design of our system, we also used a circuit simulation software package called PSpice. For the most part, the PSpice package performed our simulation tasks well; however, we were limited by the available parts in the included libraries, particularly high current solid-state switches. While many different types of transistors and thyristors were included in the libraries, none had current carrying capacities in the thousands of amps range. Consequently, many could not even crudely approximate the performance of multi-kA devices in the basic LRC circuit of our design because their resistance was too great for resonance.

Creation of our own component models appeared to be an involved process with a steep learning curve, and was judged to be out of the scope for this thesis. Since this thesis' goal is proof of concept rather than extensive modeling and simulation, we required accurate computer modeling only to the extent to which we validated the design before beginning experiment. So, to work around PSpice's limitations in validating the design, we used several different circuit simulations to approximate the actual device.

1. Low Current, Circuit Commutated

To prove to ourselves that the computer models of SCRs will actually shut off under realistic circuit-commutated conditions, we constructed a model which looks schematically nearly identical to the final experimental setup, but which used low-current thyristors. This model successfully simulated the shutoff characteristics of an SCR, but at low currents. At high currents, the resistance of the silicon devices in the counterpulsing switch was too high to allow the main bank / inductor charging circuit to resonate. So, while high currents could be forced through the model, this produced un-physical results; the SCRs used in this simulation quickly would melt. This model demonstrated the entire concept of our counter-pulsing scheme, and does so well at low currents, but it was an ineffective model for predicting the behavior of our demonstration system. It was useful in gaining a general understanding the requirements on the counterpulsing subcircuit.

2. Ideal Switch with Counterpulse Arrangement

Since we felt that we had circuit commutated turn-off well in hand, we next constructed a hybrid model to deal with the large currents of the demonstration system. We used ideal switches to test if the CP sub-circuit could force a zero-current state in the main switch leg. We used ideal closing switches in series with resistors which were valued to approximate on-state voltage drop across the NTE 5368's based upon their specifications. Since this model used ideal switches, it could not simulate turn-off, but it did give us a decent idea of the counterpulsing capacitance and charge required to force a zero-current state in the main leg.

In the end, the model showed that the CP circuit could successfully zero the current through the main switch, but beyond that provided little useful information. Without an accurate model of the actual high current SCRs used (which to our knowledge doesn't exist), simulation is not particularly useful because in our case, so much of the operation depended on the circuit-commutated turn-off time of the SCRs.

E. CIRCUIT CONSTRUCTION

Construction of the demonstrations system was fairly straightforward. The only significant problem encountered was in providing a powerful enough turn-on pulse to the SCR gate. The output of the DG-535 Delay Generator is low powered and cannot directly drive the gate. We constructed a two-channel pulse amplifier by using an in-house design. The amplifier initially was problematic but performed as designed after several internal components were replaced, resulting in an output pulse voltage of 30 V. Table 2 lists the model numbers of components used or, when no model number is available, the important characteristics of the parts.

Component	Part / Model Number / Characteristics
SCR	NTE 5368
Main Bank Capacitors	Cornell Dubilier 7P252V360N082
Counterpulsing Capacitors	Westinghouse 25 μF Maxwell 45 μF Model 37186
Diodes	International Rectifier 40HF140-ND
Main Bank Power Supply	HP6207B
Counterpulsing Power Supply	HP6209B
Storage Inductor	44 μH
Pulse Generator	Stanford Research DG-535

Table 2. Summary of Components Used

F. AS BUILT SCHEMATIC

Figure 11 is the 'As Built' schematic and an accurate representation of the electrical setup of the final experimental setup. It is also fairly representative of the physical layout of the demonstrator system. All discrete components are represented in the schematic with two exceptions: 1) the pulse delay generator and pulse amplifier are abstracted into the output of the pulse amplifiers, and 2) the three capacitors of the main bank are represented by one symbol in the schematic. Resistances internal to components are omitted for clarity, even if some values have been measured. The colors notated refer to physical terminals on the device. The Nodes marked A, B, and C are the points where voltage data displayed on oscilloscope screen-shots were measured. Figures 12 and 13 are pictures of the experimental setup.

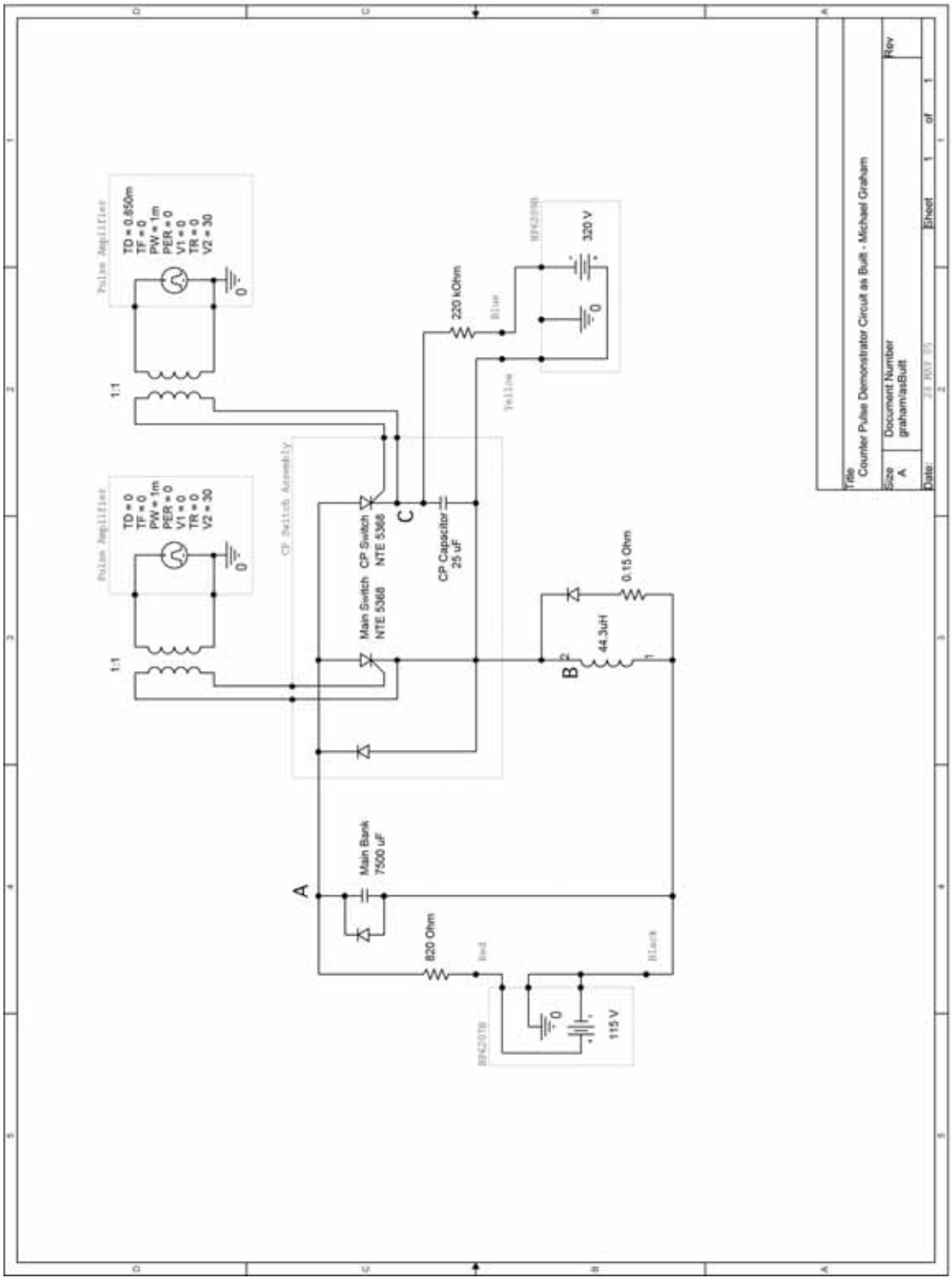

Figure 11. Counter Pulse Demonstrator Schematic As Built

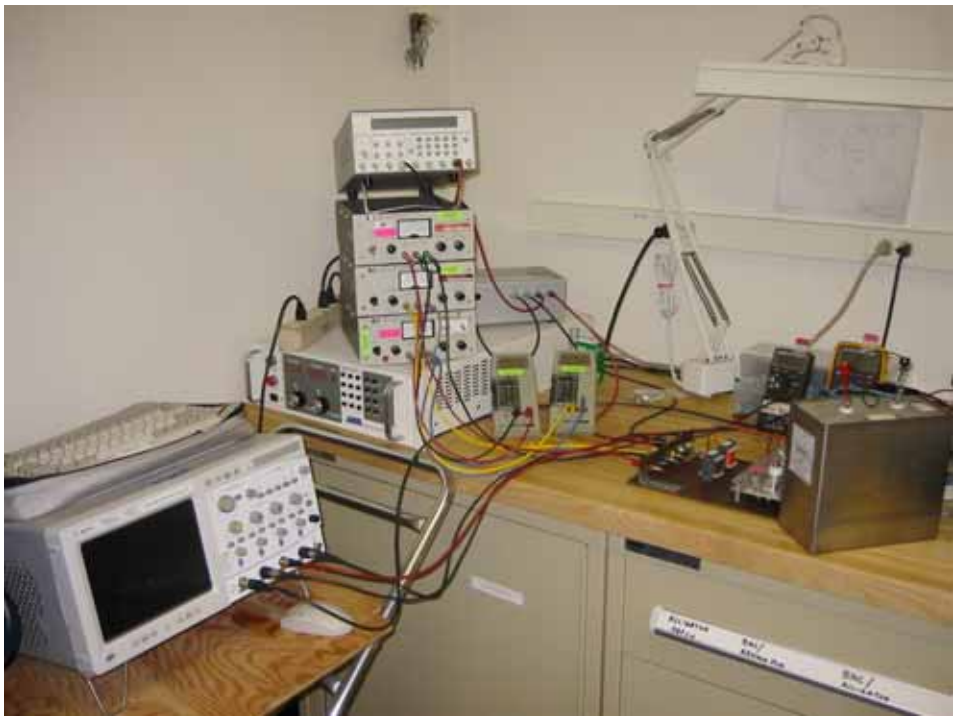

Figure 12. Picture of Experimental Setup

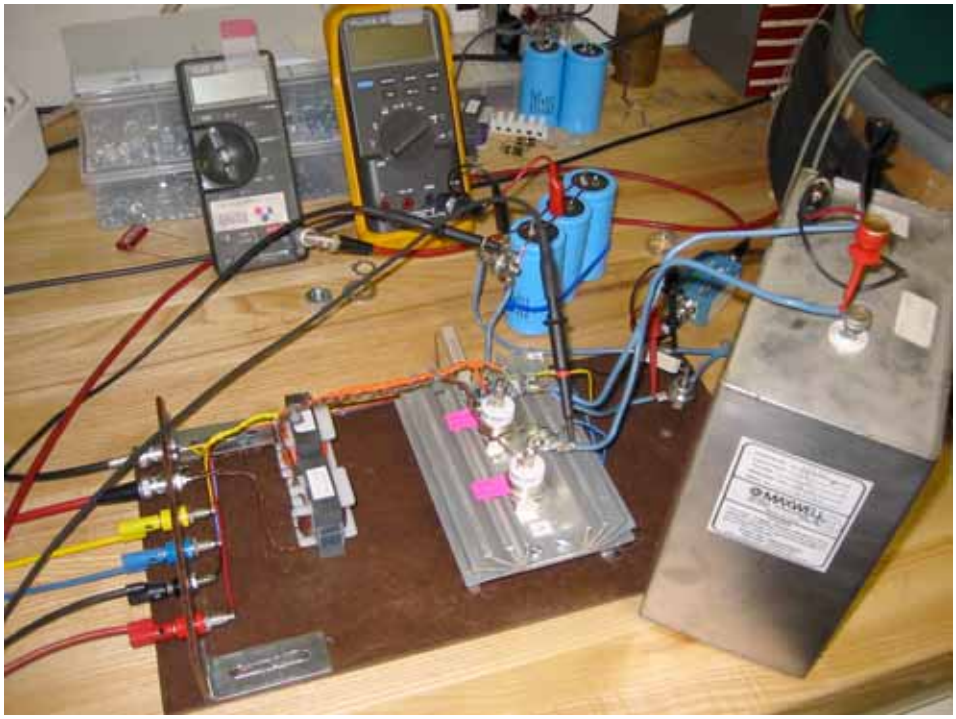

Figure 13. Close up Picture of CP Switch Assembly

III. EXPERIMENTAL RESULTS

A. SUCCESSFUL PROOF OF CONCEPT

In the original configuration, the counterpulsing demonstrator successfully interrupted 570 Amps. After increasing the counterpulsing capacitance from 25 μF to 45.6 μF, the circuit successfully achieved the design goal of interrupting 1000 Amps.

B. EXPERIMENT MECHANICS

The experimentation involved testing a variety of peak current and initial charge on CP capacitor combinations. Varying the initial charge on the main capacitor bank controlled the peak current in the LC inductor charging circuit. Changing the initial voltage across the CP capacitor varied initial charge on the counterpulsing capacitor. Initial voltages on both banks were set using Fluke multimeters. Current through the inductor (the current at point B in Figure 11) was observed by means of a Pearson Model 1330 Pulse Current Monitor placed around one inductor lead. This Current Monitor had a sensitivity of 0.005 V/A. Voltage probes with division factors of 10:1 were used to observe the voltages across the main bank and the voltage of the CP switch cathode (the voltages at points A and C). The voltage across the inductor (the voltage at point B) was measured with a 101:1 resistive divider. All four inputs were recorded on a Agilent Infiniium 4-channel Oscilloscope. Figure 14 is an oscilloscope screen shot, showing voltages at points A and B and current at Point B, typical of a successful CP switch opening. See Table 3 for a summary of channel division factors. The Appendix displays an unsuccessful shot.

The differences between waveforms of a successful switch opening and a failure were easy to note. The most obvious difference is shown in the inductor voltage trace (Channel 3 in Figure 14). When the CP switch fails to open, the inductor voltage fails to go negative. Secondly, the shape of the inductor current after switch opening has a much steeper decay than that of an LCR tank circuit, which is what the system behaves like if the switch fails to open. Thirdly, the sound of the inductor coils tightening upon each

other is noticeably different because of the faster discharge time – a successful switch-opening event sounds much sharper and metallic than a failure and subsequent LCR discharge.

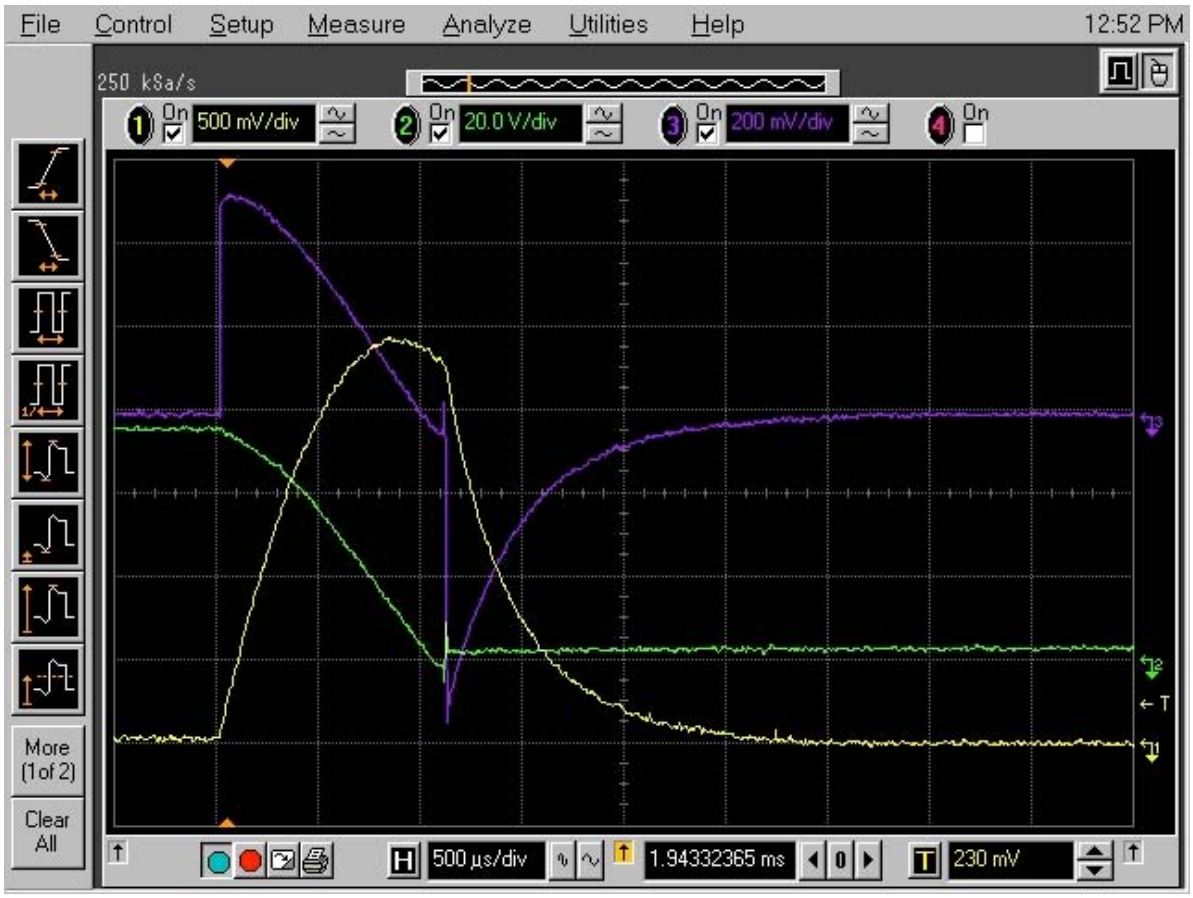

Figure 14. 1 kA Interruption Oscilloscope Screenshot; see Table 3 for Parameters

Ch	Color	Division Factor	Location on Fig. 11	Quantity
1	Yellow	0.005 V/A	Current at B	Inductor Current
2	Green	10:1	Voltage at A	Main Bank Voltage
3	Purple	101:1	Voltage at B	Inductor Voltage

Table 3. Trace Parameters from Figure 14

C. ORIGINAL CONFIGURATION: 25 µF CP CAPACITOR

In the original configuration with the 25 µF counterpulsing capacitor, the system was tested over a range of maximum interruption currents between 400 A and 570 A. The delay between main switch close and CP switch close was varied between 1.00 ms

and 1.15 ms. The switch worked best at 1.10 ms of delay between pulses. Initial voltage on the main bank varied between 60 and 70.2 volts and initial voltages on the counterpulsing capacitor varied between 250 and 310 volts. Above approximately 570 A of peak current, the counterpulsing switch failed to open regardless of the initial voltage on the counterpulsing capacitor. Because of this observation, I increased the capacitance of the counterpulsing capacitor.

D. MODIFIED CONFIGURATION: 45.6 μF CAPACITOR

I increased the capacitance by replacing the 25 μF CP capacitor with a Maxwell 45 μF Capacitor, Model 37186 whose capacitance I measured at 45.6 μF using an ESI Model 252 Impedance Meter. After the change, the system successfully interrupted a current of 1kA. For the 1kA peak current trial, the main bank was charged to 110 V and the CP bank held an initial charge of 326 V. Figure 14 is the screenshot of this trial and Table 4 summarizes the initial voltages and charges.

Peak Current Interrupted	1000 A
Initial Main Bank Voltage	110 V
Initial Main Bank Charge	0.825 C
Initial CP Voltage	326 V
Initial CP Charge	0.015 C

Table 4. Summary of 1 kA Trial Parameters

E. TIMING SENSITIVITY

The timing of the counter-pulse operation proved to be critical to switch opening. In hindsight, the design goal of a 1 ms inductor charging time was a good choice. Based on experiment, the most successful time to trigger the CP switch close was at the zero main bank voltage point, which occurred in our case at 1.1 ms after main switch closing. From an ideal standpoint, the best time for current interruption is at maximum current, since the voltage generated by the inductor is zero. But the demonstration system has enough resistance internal to the capacitor bank and switching system that it does not

behave ideally. In practice, the main bank zero-voltage time is far more effective for CP switch operation. A decrease in delay 50 μs from 1.05 ms to 1.00 ms consistently caused the switch to fail. CP switches, particularly those using circuit-commutated devices, are relatively intolerant of timing errors. A decrease corresponding to 5% of charge time makes the difference between successful operation and failure. The switch proved somewhat more tolerant of increases in delay time; it worked roughly half the time when a delay of 1.10 ms was used.

IV. DISCUSSION

A. PRIMARY ISSUES ENCOUNTERED

Various minor issues occurred during the construction and testing of the demonstration circuit. Several isolation resistors melted due to operator error involving current limits on power supplies. One of the SCRs developed a short for unknown reasons and was replaced. Experimentation was without major difficulty overall and switch performance was as expected.

B. UNDERSTANDING OF CP SWITCH OPERATION

Figures 15 and 16 show plots of initial CP voltage (V_{cp}) vs. maximum interrupted current (I_L) for the 26.4 μF and 45.6 μF CP capacitors respectively. Initial CP charge (Q_{cp}) vs. maximum interrupted current (I_L) for both capacitors are displayed in Figure 17. The data for the 26.4 μF capacitor is particularly noisy. I attribute some of this to intentional variations in CP timing, and some to operator error; I determined after the fact that some trials may not have begun with the full CP voltage indicated. However, the data still seems to indicate an upper bound on interruptible current for this CP capacitance. Figure 16 suggests an exponential dependence between V_{cp} and I_L, but both linear and exponential fits to this data are equally poor so I omit them in the figure.

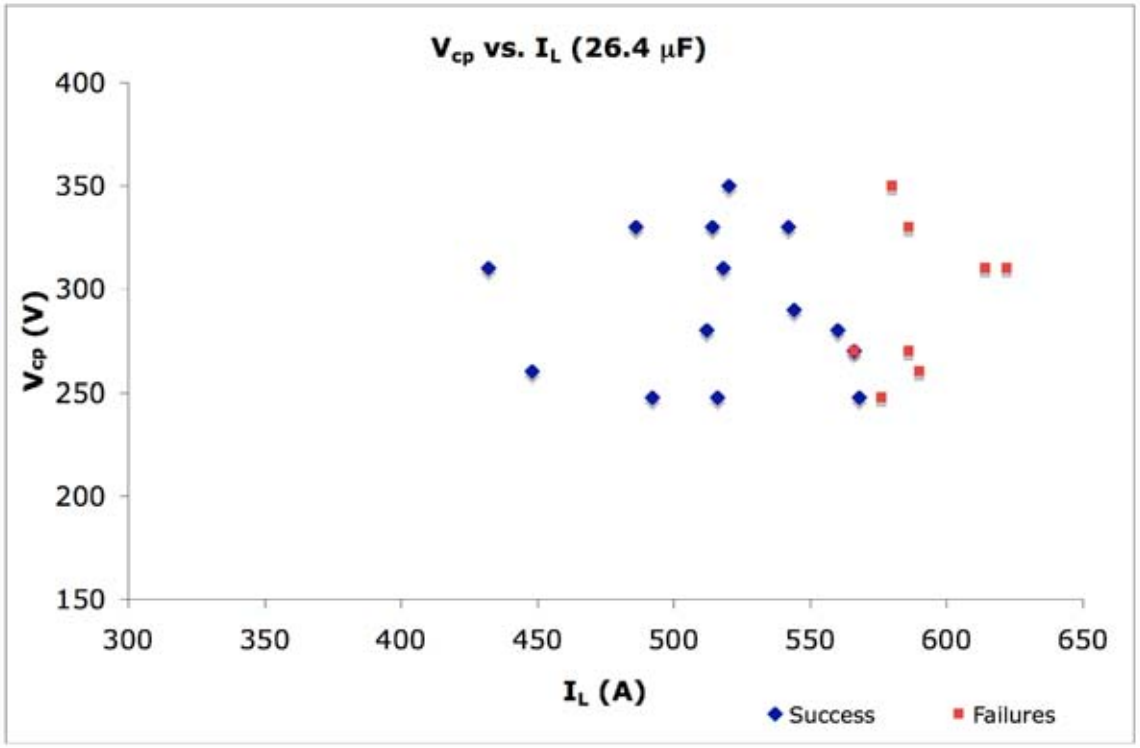

Figure 15. Results for 26.4 mF Capacitor

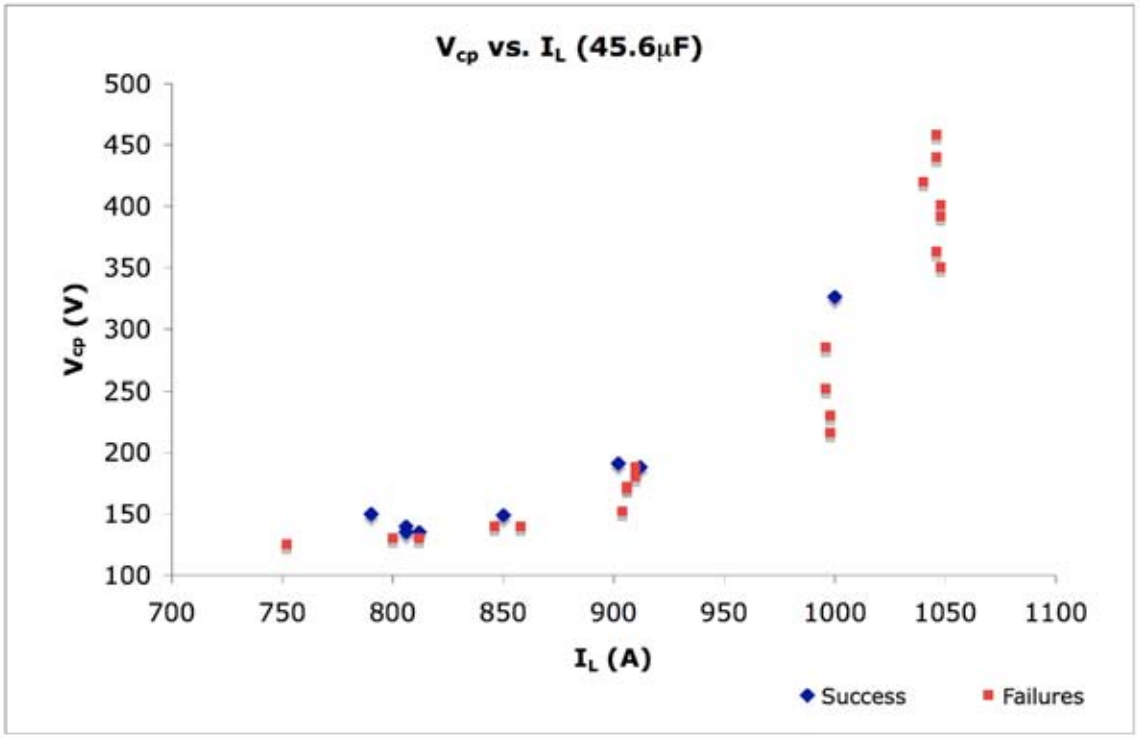

Figure 16. Results for 45.6 mF Capacitor

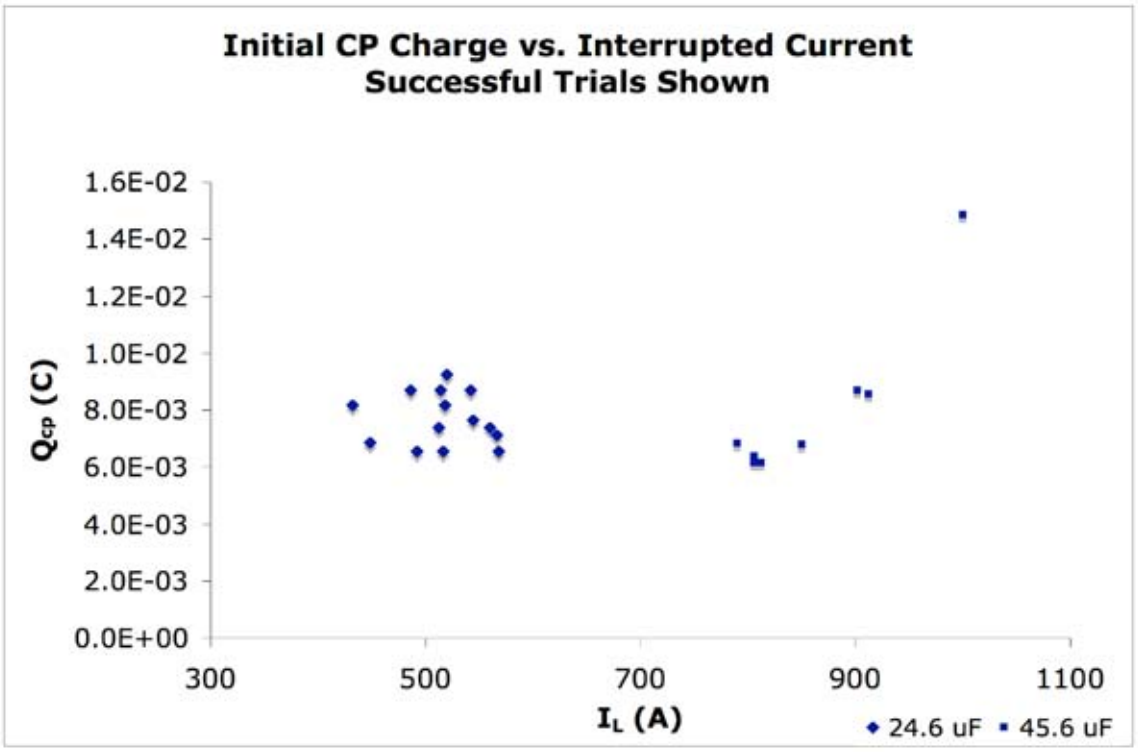

Figure 17. Combined Results for both CP Capacitances

The inconclusive nature of the data with respect to establishing a relation between V_{cp} and I_L are disappointing, but goal of concept was still successful. We are not particularly concerned for two reasons: the devices used in the 250 kJ system will be a different type, so any precise relation would be inapplicable; and the circuit commutated turn-off time is not precisely specified, so the variation in results is expected since we depend on circuit commutated turn-off for the demonstration system's operation. The result that the system reaches an upper limit of maximum turn-off current that appears to be independent of Q_{cp} charge suggests that the relation between turn-off current and capacitance is more important than the relation between turn-off current and CP stored energy. In any case, further investigation will be necessary with the components of the 250 kJ system before it is run at full current.

C. BUILD PLAN FOR 250 KJ SYSTEM

One of the major initiatives of the railgun research group is a modular PFIN system employing solid-state opening switches. Our work indicates that a counterpulsed solid-state switch is a viable means of achieving this design goal. Schematically, one module of the 250 kJ system will look very much like the current demonstrator system,

with the scale increased by a factor of 50. Functionally, the design will differ in one major respect: instead of using circuit commutated shutoff devices (e.g. SCR) like this demonstrator, the 250 kJ system will use Integrated Gate Commutated Thyristors, which are gate commutated shutoff devices.

Since the semiconductors will be of a different type in the 250 kJ system, the turnoff characteristics of the devices will be not only a function of the current through the cathode, but also a function of the gate shutoff. This characteristic will make timing a more crucial issue for the larger, modular system. On the other hand, the requirements on the counterpulsing system will be less demanding; in our demonstration system, the counterpulsing system was required to hold the current through the main switch for several tens of microseconds in order for the main switch to commutate to off state. In our larger system, the counterpulsing system will only be required to reduce the current through the main switch from 50 kA to below 4 kA, rather than to force the current to zero.

D. CONCLUSION

We showed that counterpulsing techniques can successfully turn-off currents on the order of 1 kA. This thesis was successful with respect to its own goal, but we still must demonstrate counterpulsing at higher currents in order for the concept to be useful in a railgun-class PFIN. Nevertheless, our early success bodes well for the larger system currently planned.

APPENDIX

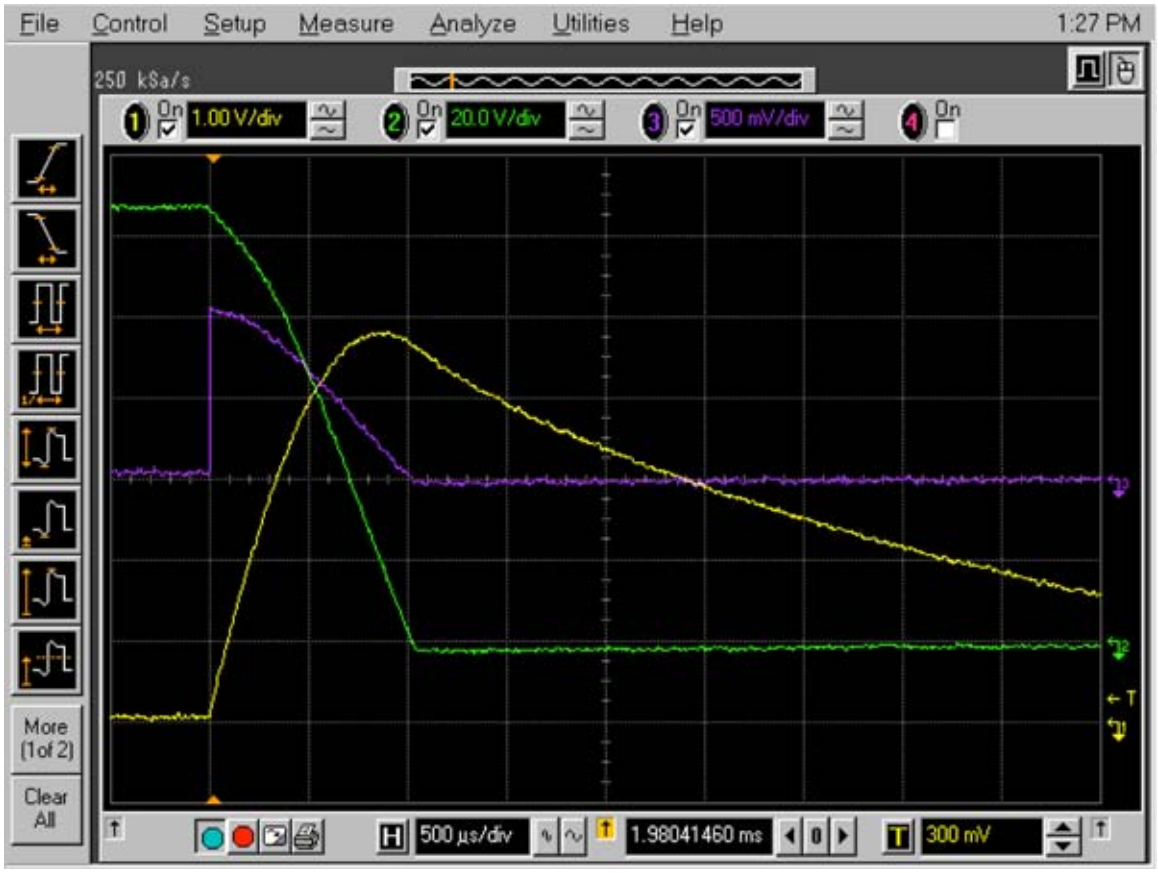

Figure 18. CP Switch Failure-to-Open: Oscilloscope Screenshot. See Table 3 for Parameters

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